Introduction

The EG&G Reticon K Series linear photodiode arrays are designed for applications that require higher sensitivity and wider dynamic range than is available with square element geometries. Devices in this series contain 128, 256, 512 or 1024 photodiodes on 25 µm centers. Typical applications include HPLC, conventional spectroscopy, and noncontact measurement in robotics and factory automation.

Key Features

- 128, 256, 512 or 1024 elements
- Wide 250 µm aperture for higher sensitivity
- Single-phase TTL clock (open collector TTL or 5V CMOS)
- On-chip driver
- Differential output for on-chip noise cancellation

Packaging

Devices are packaged in 16, 18 or 22-pin dual-inline IC packages with ground and polished quartz windows. The pinout configurations are shown in Figure 1 and package dimensions are shown in Figure 11.

General Description

The devices consist of a row of silicon photodiodes, each with an associated junction capacitance on which to integrate photocurrent, and a multiplex switch for periodic readout via an integrated shift register scanning circuit. The shift register clock driver is also integrated so that only a single-phase TTL clock is required for scanning. A row of dummy diodes is read out differentially with the active photodiodes to allow cancellation of multiplex switching transients and to provide a clean video signal with a minimum of external circuitry.

A simplified equivalent circuit of a K Series photodiode array is shown in Figure 2.

Each cell consists of an active photodiode and a dummy photodiode, both with an associated junction capacitance. These diodes are connected through MOS multiplex switches to active video and dummy video recharge lines that are common to all the cells. The switches are sequentially closed for one clock period by the shift register scanning circuit, thereby recharging each cell to 5V and storing a charge of approximately 4 pC on its capacitance. The scanning circuit is driven by a single-phase dynamic shift register (actually two registers in parallel, one for even-numbered diodes and the other for odd-numbered diodes) and a drive circuit which generates four clock phases and two properly-timed start pulses to load the two registers. The individual cells are actually interdigitated with the odd elements being sampled by one register and the even-numbered cells by the other register.

NEG Supply	1	16	Clock
Start	2	15	NC
NC	3	14	Ground
NC	4	13	NC
POS Supply	5	12	End of Scan
Buffer Supply	6	11	Dummy Recharge
Video Recharge	7	10	Recharge Gate
Video Buffer	8	9	Dummy Buffer

RL0128K & RL0256K

NEG Supply	1	18	NC
Start	2	17	Clock
NC	3	16	Ground
POS Supply	4	15	POS Supply
Buffer Supply	5	14	End of Scan
NC	6	13	NC
Video Recharge	7	12	NC
Video Buffer	8	11	Dummy Recharge
Dummy Buffer	9	10	Recharge Gate

RL0512K

NEG Supply	1	22	NC
Start	2	21	Clock
NC	3	20	NC
NC	4	19	NC
NC	5	18	Ground
POS Supply	6	17	POS Supply
Buffer Supply	7	16	End of Scan
NC	8	15	NC
Video Recharge	9	14	NC
Video Buffer	10	13	Dummy Recharge
Dummy Buffer	11	12	Recharge Gate

RL1024K

Figure 1. Pinout Configurations

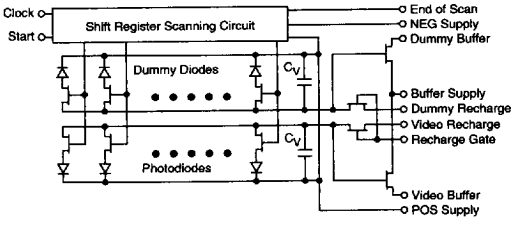

Figure 2. Simplified Equivalent Circuit

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The cell-to-cell sampling rate is the clock frequency, and the integration time is the interval between start pulses. During this line time, this charge stored on each photodiode is gradually removed by photocurrent. The photocurrent is the product of the diode sensitivity and the light intensity or irradiance. The total charge removed from each cell is the product of the photocurrent and the line time. This charge must be replaced through the video line when the diode is sampled and reset once each scan.

In addition to the signal charge, switching transients are capacitively coupled into the active video line by the multiplex switches. Similar transients are introduced into the dummy video line and therefore can be reduced (and a cleaner signal recovered) by reading out the active video and dummy video lines differentially.

In many applications, the recharge gate is biased to the negative supply potential and an output signal is obtained simply by differentially amplifying the recharge pulses on the active video and dummy video recharge lines. However, internal buffer amplifiers that are also provided may be used as part of a sample-and-hold video output circuit.

Sensor Geometry

In the K line scanners, the light-sensing area is a long, narrow rectangular region defined by an aperture in an opaque mask. Bar-shaped photodiodes extend across the aperture and are connected to the multiplex switches buried under the mask. The entire aperture is photosensitive; photocurrent generated by light incident between the photodiodes will be collected by the nearest diode. Figure 3 shows the aperture geometry along with an idealized response function that would be obtained by scanning a point source of visible light along the length of the aperture. The dimensions *a*, *b*, and *c* in Figure 3 are as follows: the photodiode width *a* is 15 µm, the center-to-center spacing *b* is 25 µm, and the aperture width *c* is 250 µm.

Sensitivity and Spectral Response

The spectral response of the K Series devices is similar to that of other high quality silicon photodetectors, covering the range from near UV to the near IR. A standard quartz window assures a full spectral bandwidth. Relative spectral response is shown as a function of wavelength in Figure 4. Note that a smooth spectral response down to the UV is maintained, unlike CCDs, which use a polysilicon layer over the photosite and thus have no response in the UV.

Since Reticon photodiode arrays operate in the charge storage mode, the charge output of each diode (below saturation) is proportional to exposure; i.e., the irradiance or light intensity multiplied by the integration time or the time interval between successive start pulses. Thus, there is an obvious trade-off between scanning speed and the required light intensity. A plot of charge output versus exposure is shown in Figure 5.

Uniformity of response along the length of a photodiode array is a function of wavelength. Devices tend to be less uniform at long wavelengths (IR) and more uniform at short wavelengths (visible).

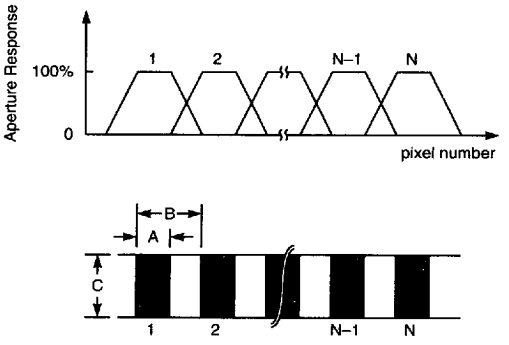

Figure 3. Sensor Geometry and Idealized Aperture Response Function

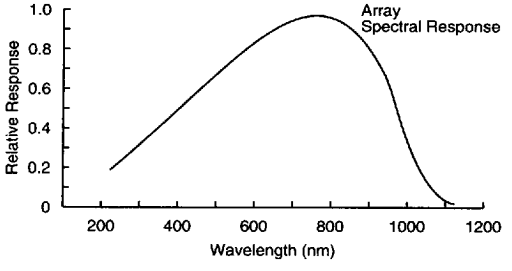

Figure 4. Relative Spectral Response as a Function of Wavelength

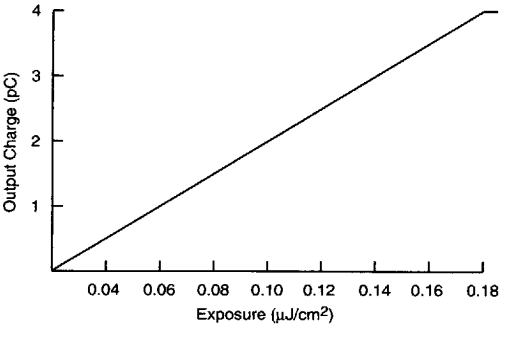

Figure 5. Signal Charge Per Cell as a Function of Exposure (Light Intensity x Line Scan Time)

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Dark Response and Dynamic Range

There are three components in the dark output signal from a Reticon line scanner: (1) the integrated dark leakage current; (2) the fixed pattern noise caused by incomplete cancellation of clock switching transients which are capacitively coupled into the video line, and (3) the random pixel noise.

The dark leakage current will vary from element to element but is typically less than 2 pA at room temperature. Assuming this value, leakage current would contribute an output charge of 2 pC with a 1 sec line time, or .08 pC with a 40 ms line time. Thus, since the saturation charge is typically 4 pC, dark current will contribute about 2% of the saturated output signal for t_L = 40 ms, 0.2% for t_L = 4 ms, and so on. The dark current is a very strong function of temperature, approximately doubling for every 7°C increase of photodiode temperature. Thus, the maximum allowable line time becomes correspondingly shorter at high temperatures, and longer at low temperatures. An important feature of the K device design is its low power dissipation, which means that self-heating is negligible. Dark current does not become a limiting factor in the dynamic range unless very long integration times or highly elevated temperature are used.

The switching noise appears as a fixed pattern which is spatially random except that it may have a slight 1, 2, 3, 4 pattern because alternate diodes are sampled on different phases of an internally-generated, four-phase clock. Fixed pattern noise is largely removed by differential readout; its residual amplitude will typically be 1% of the saturation level at a 40 ms integration time.

Pixel noise is the random, nonrepetitive fluctuations superimposed on the dark level and is the ultimate limiting noise that cannot be removed by signal processing. Its rms value will generally be amplifier-limited at a value less than about 0.1% of the saturation level, depending on the noise bandwidth and preamplifier used.

The dynamic range that can be achieved depends on circuit complexity and layout techniques. Care must be exercised in circuit layout to provide for adequate ground plane, circuit decoupling, and avoidance of electrostatic pickup.

Drive Requirements

Two power supplies to the array are required—nominally +5 and -10V. The clock and start timing signals may be at TTL level, and may be supplied from other parts of the system or generated by using a simple circuit such as that shown on Figure 6. In this circuit, the start pulse is obtained by counting clock pulses. By setting the appropriate switches, the number of clock periods, n, between start pulses may be set at any desired value greater than or equal to N, the number of elements in the array. However, the total time between start pulses $t_L = n/f_S$ should not exceed approximately 40 ms (at room temperature) to prevent integrated dark current from making a significant contribution to the output charge.

A timing diagram showing the relationship between the clock and start pulses and the video and end-of-line outputs is shown in Figure 7.

Signal Extraction

The video output of the K devices is a train of N charge pulses flowing onto the video recharge line and dummy recharge line capacitances during each scan, with timing as shown in Figure 7. The pulses on the dummy line contain switching transients only; those on the video line contain switching transients plus the video signal. An output circuit is required which is capable of differentially amplifying these pulses to a useable voltage level.

An integrated sample-and-hold amplifier similar to the type used on Reticon's evaluation board is recommended for the best signal-to-noise ratio performance.

The signal processing scheme makes use of the internal buffer amplifiers and recharge switches. Immediately after the multiplex switch is closed to sample a diode, the voltage change on the video line is sensed through the buffer amplifier, and sampled and held. The recharge gate is then pulsed negative to reset the video line before the next diode is sampled. The result is a sampled and held boxcar video signal such as that shown in Figure 8. Timing and circuitry for this mode is shown in Figures 9A and 9B.

End-of-Scan

An output pulse is provided when the next-to-last element is sampled by the shift register scanning circuit. This end-of-scan output is provided primarily for test purposes. When not in use, it should be connected to the positive supply to avoid introduction of unwanted "glitches" into the video. In some applications, however, it may be desirable to use the end-of-scan output. In these cases, it is recommended that the voltage excursion on the end-of-scan terminal be minimized by using a circuit such as that shown in Figure 10.

Evaluation Boards

Evaluation circuitry containing all the required drive and amplifier circuitry for the operation of the K Series is available from Reticon. These circuits are highly recommended for first-time array evaluation. In many cases, they are also useful for design into final equipment.

RC0100B Series

These circuits provide an integrated, sampled-and-hold-boxcar output as shown in Figure 8. Each circuit is divided into two boards—a standard "motherboard" which contains most of the circuitry, and a small "array board" which contains only those components which must be located close to the array. The array board may be plugged directly into the motherboard or can be extended up to 30 inches away via an optional ribbon cable.

The motherboard (RC0100LNB) is 4.5 x 6.5 inches in size and is terminated by a standard 22-pin edge connector. The array boards (RC0104N, etc.) are 3 inches square and have mounting holes in each corner on 2.6-inch centers. A different array board is required for each array type.

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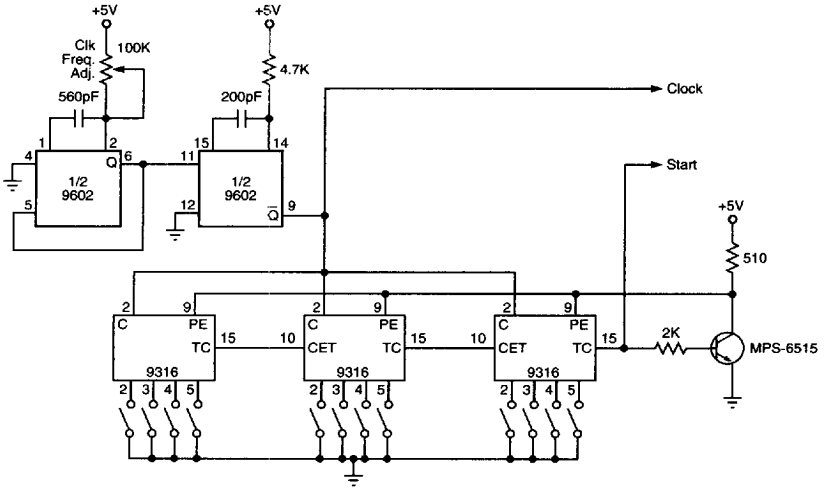

Figure 6. Clock and Counter Circuit Suitable for Generating TTL Clock and Start Pulses

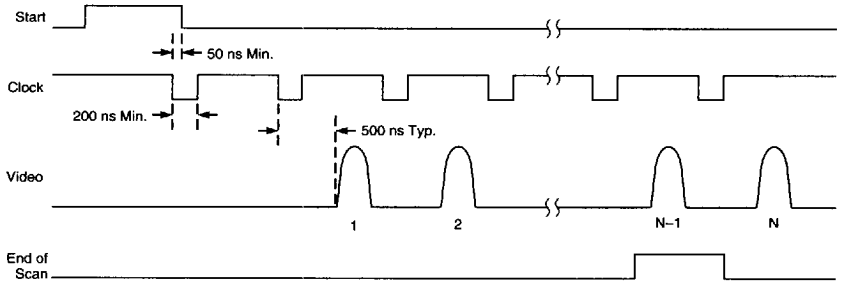

Figure 7. Recharge Mode Timing Diagram

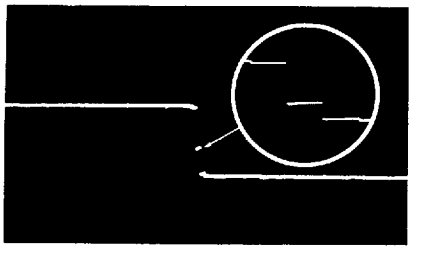

Figure 8. Oscilloscope Photograph Showing Video Output of Integrate, Sample-and-Hold Amplifier

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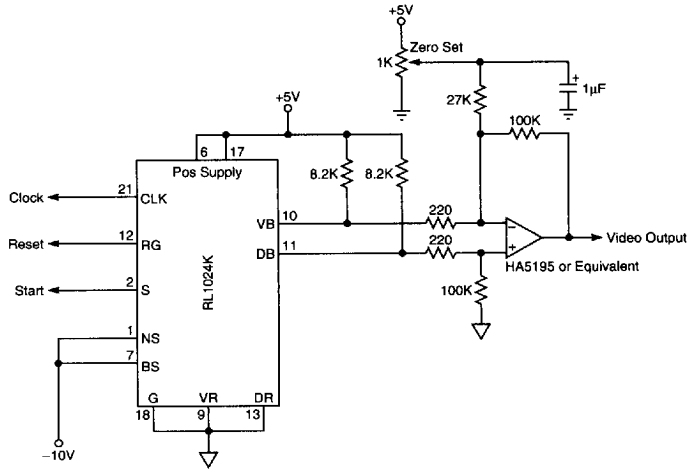

Figure 9A. Buffer Mode Operation Simplified Diagram

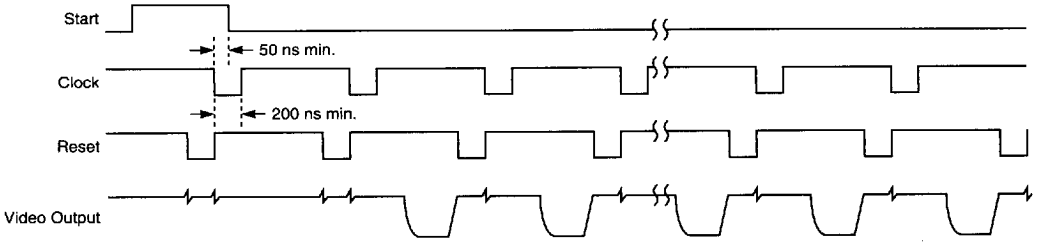

Figure 9B. Buffer Mode Timing Diagram

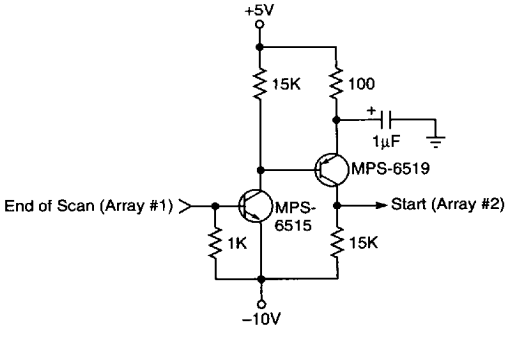

Figure 10. End-of-Scan Output Circuit Suitable for Generating Start Pulse for a Second Array

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Table 1. Electrical Characteristics (25°C)

	Min	Typ	Max	Units
Positive supply voltage V_P [1]	+4.5	+5	+5.5	V
Negative supply voltage V_N	-10.5	-10	-9.5	V
Clock voltage low V_{CL}	-10.5	0	+1	V
Clock voltage high V_{CH}	V_P-1	+5	V_P	V
Start voltage low V_{SL}	-10.5	0	+1	V
Start voltage high V_{SH}	V_P-1	+5	V_P	V
Recharge gate voltage low V_{RL}	-10.5	-10	-9.5	V
Recharge gate voltage high V_{RH}	V_P-1	+5	V_P	V
Clock pulse width	0.2	-	-	µs
Start pulse width		See Figure 7		
Clock frequency f_c	-	-	1	MHz
Integration time t_i [3]	-	-	40	ms
Clock input capacitance C_c [2]	-	4	-	pF
Start input capacitance C_s [2]	-	4	-	pF
Video line capacitance C_v [2]				
RL0128K	-	8	-	pF
RL0256K	-	12	-	pF
RL0512K	-	20	-	pF
RL1024K	-	30	-	pF
End-of-scan output resistance	-	5	-	KΩ
DC power dissipation [4]	-	45	-	mW

Notes:

1 No terminal should ever be allowed to go more positive than V_P
2 Measured with nominal power supply voltages
3 Integration time can be longer if the array is cooled and/or if the application can tolerate a larger percentage of dark signal.
4 Mostly due to use of on-chip buffers. When recharge mode is used (buffers biased off), power dissipation is on the order of 1 mW.

Table 2. Electro-Optical Characteristics (25°C)

	Min	Typ	Max	Units
Diode center-to-center spacing	-	25	-	µm
Diode aperture width	-	250	-	µm
Photodiode sensitivity [1]	-	25	-	pC/µJ/cm^2
Nonuniformity of sensitivity [1]				
RL0128K	-	7	10	±%
RL0256K	-	7	10	±%
RL0512K	-	9	11	±%
RL1024K	-	12	14	±%
Saturation charge	-	4	-	pC
Saturation exposure		0.18		µJ/cm^2

Note:

1 Measured using a 2870°K broadband light source filtered with a Fish-Schurman HA-11 heat absorbing filter. The first 2 and the last 2 diodes are neglected

Absolute Maximum Ratings

	Min	Max	Units
Voltage on any terminal	V_P-20	V_P	V
Storage temperature	-55	+125	°C
Temperature under bias	-55	+85	°C

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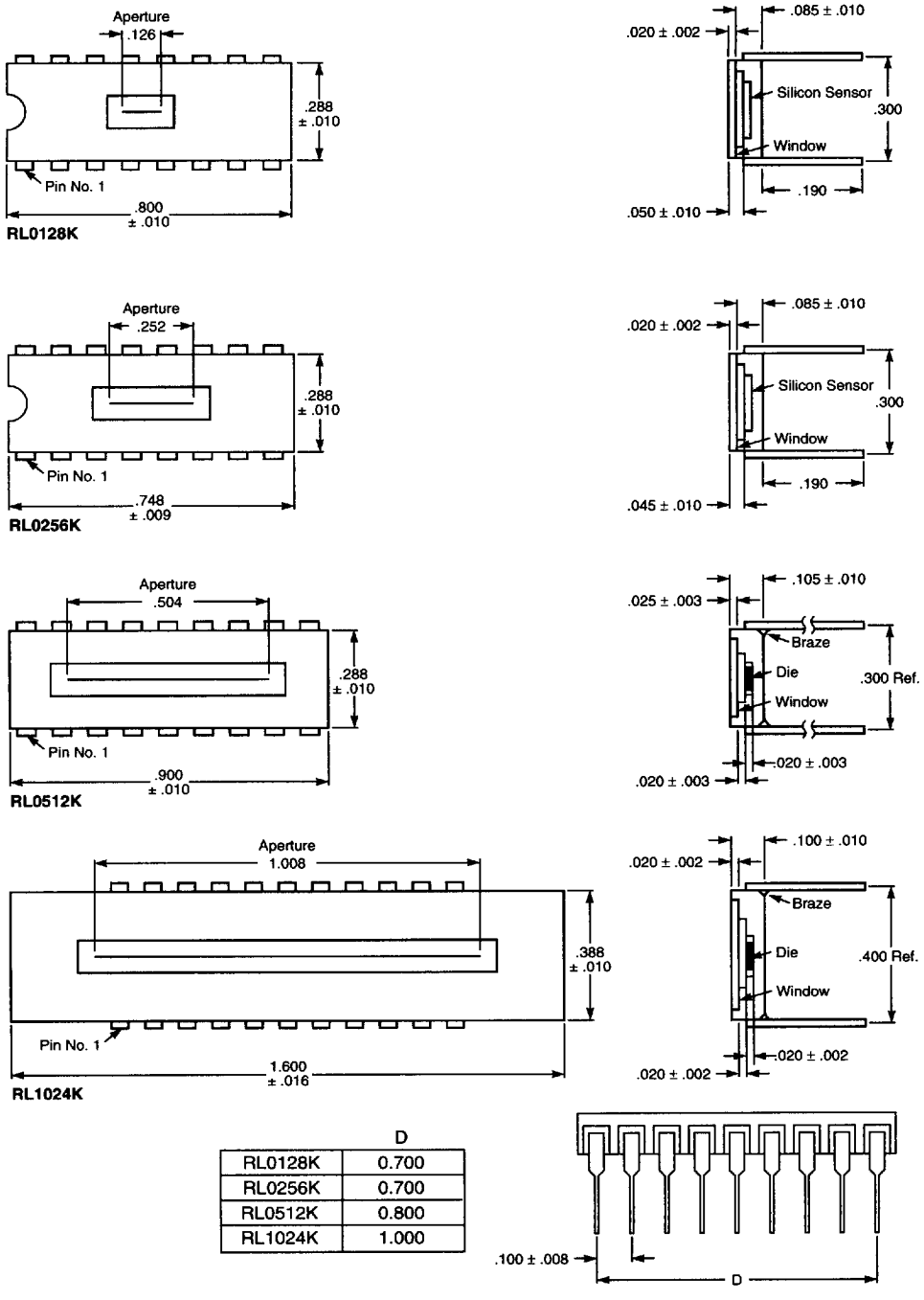

	D
RL0128K	0.700
RL0256K	0.700
RL0512K	0.800
RL1024K	1.000

Figure 11. Package Dimensions

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Ordering Information *

Part Number	Evaluation Circuit	
	Current Amplifier	Integrate, S/H Amplifier
RL0128KAQ-011	RC0301LNN-011	RC0100LNB-011/RC0104LNN-011
RL0256KAQ-011	RC0301LNN-011	RC0100LNB-011/RC0104LNN-011
RL0512KAQ-011	RC0302LNN-011	RC0100LNB-011/RC0105LNN-011
RL1024KAQ-011	RC0303LNN-011	RC0100LNB-011/RC0106LNN-011

* For standard devices. For options, consult your local sales offices.

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